(19) Europäisch s Patentamt
European Patent Office
Office uropéen des brevets

(11) EP 1 109 349 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
20.06.2001 Bulletin 2001/25

(51) Int Cl.[7]: **H04L 7/00**, H04L 12/56, H04J 3/06

(21) Application number: **00311217.4**

(22) Date of filing: **15.12.2000**

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE TR
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **17.12.1999 GB 9929769**

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(54) Clock recovery pll for ATM networks

(57) The invention relates to packet switched networks. and more particularly to a circuit and a method for clock recovery in cell-relay networks, particularly ATM (Asynchronous Transfer Mode) networks offering constant bit rate services. The multimode clock recovery circuit has an embedded digital phase locked loop including an input circuit capable of generating a phase signal from at least two types of input signal. The phase signal controlling the output of the phase locked loop generates clock signals for the constant bit rate services.

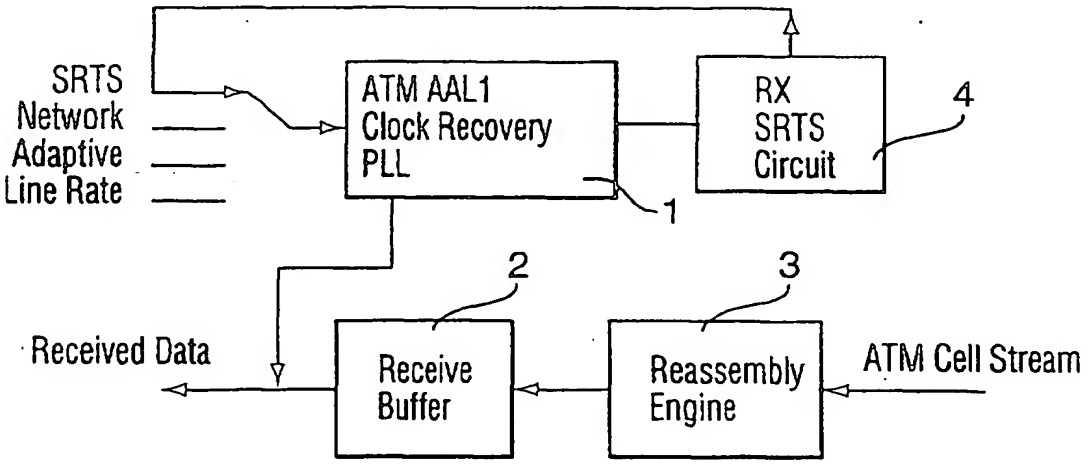

FIG. 3

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[0014] In the Line Rate mode. the PLL to go into accurate holdover mode when the input data link is determined to be in Loss Of Synchronization state.

[0015] When the Dynamic Bandwidth Circuit Emulation Services is used with Adaptive mode. and all DSO channels are disconnected (the all-idle state). only a few cells are transmitted each second to keep the ATM link alive. but no TDM (Time Division Multiplexed) bytes are transferred. The clock recovery circuit of the invention will automatically go into accurate holdover mode when the all-idle state is detected as defined by the DBCES channel activity bit mask.

[0016] The invention can also provide an accurate freerun clock (0.1 ppm with an accurate MCLK master clock). reduced output jitter, large input jitter acceptance (configurabie in gates). It also performs SRTS for UDT (standardized) and also SRTS for SDT (non-standard).

[0017] The ability to do Line Rate and SRTS Clocking in one PLL means that at the transmitting end the present invention can be used to de-jitter the incoming clock before it is used to generate SRTS time stamps, and at the receiver another instance of the present invention can be used to generate the outgoing clock from the SRTS. This is important, because the sampling effects of the time stamp process will alias the jitter frequencies downward, where they will be harder to filter for the receiver PLL (creating wander).

[0018] The invention will now be described in more detail, by way of example only. with reference to the accompanying drawings, in which;-

Figure 1 is a block diagram showing adaptive line rate clocking;

Figure 2 is a block diagram showing adaptive clock recovery;

Figure 3 is a block diagram showing SRTS clock recovery;

Figure 4 is a block diagram showing normal transmit SRTS;

Figure 5 is a block diagram showing transmit SRTS de-jittering;

Figure 6 is a block diagram of the digital PLL;

Figure 7 is a block diagram of the SRTS generator;

Figure 8 is a block diagram of the phase detector for SRTS inputs;

Figure 9 is a block diagram of the phase detector for clock inputs:

Figure 10 shows a combined phase detector for both kinds of inputs:

Figure 11 is a block diagram of the loop filter;

Figure 12 is a block diagram of the digital controlled oscillator; and

Figure 13 is a block diagram of the jitter reduction circuit;

[0019] In Figure 1. the digital phase locked loop (PLL) 1 receiving a line rate input clocks received data out from receive buffer 2. The incoming ATM cell stream is reassembled in reassembly engine 3.

[0020] In the adaptive scheme shown in Figure 2, buffer fill-level information is returned from the receive buffer 2 to the input of the PLL 1.

[0021] In the SRTS scheme shown in Figure 3, the receive SRTS circuit 4 recovers timing information from the incoming time stamps and provides an input to PLL 1.

[0022] In Figure 4, the line rate input is fed to transmit SRTS circuit 6, which generates residual time stamps to be included in the cell stream by segmentation engine 5.

[0023] By including the clock recovery PLL, as shown in Figure 5, the circuit can be used to de-jitter an incoming clock before it is used to generate SRTS time stamps, and at the receiver another instance of the circuit can be used to generate the outgoing clock from the SRTS. This is important because the sampling effects of the time stamp process alias the jitter frequencies downward, where they are harder to filter for the receiver PLL, which creates wander.

[0024] As noted above, the PLL 1 operates in the following modes:

- Synchronous mode: The PLL synchronizes to the incoming clock.

(continued)

Relevant Specifications			
Clock	Electrical	Jitter	Wander
E1	ITU-T G.703	ITU-T G.823	ITU-T G.823
J2	ITU-T G.703	ANSI DSI.102 JT-G.703a	JT-G.703a,

[0031] Jitter transfer functions are not specified in the above standards. However, some ITU-T specs. regarding digital multiplex equipment, such as G.743, specify jitter transfer functions. For the MT9042, the requirement is that the jitter transfer corner frequency be between 1.2 and 2.0 Hz (ETSI spec.), with a 20 dB/dec roll off. This range is used for this PLL for all input frequencies and meets the requirements of G.743. The jitter transfer is less than +0.5 dB.

[0032] The standards from the above Table specify wander/jitter input tolerance and maximum output jitter. For the input wander/jitter tolerance, the low frequency parts are the largest and are therefore the most important for the PLL requirements (see the Table below). With a corner frequency larger than 1.2 Hz, it is assumed that the PLL follows wander below 0.1 Hz. The range of the phase detector is therefore based upon the wander tolerance at 0.1 Hz and is 32 UI peak-to-peak (+/- 16 UI).

Minimum Input Wander and Jitter Tolerance				
Clock	A0[Ui_{pp}]	A1[Ui_{pp}]	F0[Hz]F1 [Hz]@0.1Hz[UI_{pp}]	
DS1	28	5	1.2E-5 10	6.2
E1	37	18	1.2E-5 20	23
J2	114	5	1.2E-5 10	15

[0033] The maximum output jitter on the output of the PLL as specified in the appropriate standards is listed in the Table below.

Maximum Allowed Output Jitter		
Clock	A[UI_{pp}]	A[ns]
DS1	0.07	45
E1	0.2	98
J2	0.1	16

[0034] ANSI DS1.403 and DS1.101 require that the output phase change no more than 81 ns per 1.326 ms. The maximum allowable output phase shift with respect to the ideal reference source is 1 µs. Therefore, the slew rate of the DCO input may be no more than 61 ppm of the center frequency setting. The "no more than 81 ns / 1.326 ms" requirement is met for all modes.

[0035] Because the period of the E1/DS1/J2/C4/C8 signals is less than 1 µs. that requirement is met automatically when the PLL is in synchronous mode. When switching between modes, the 1 µs MTIE is not met.

[0036] The SRTS generator 14, shown in Figure 7, is the same as the standard solution indicated in ITU standard 1.363.1 and described US patent 5,260,978, which is simple, small and efficient. In master mode, the SRTS generator is needed to generate an RTS (residual time stamp) that is transmitted. In slave mode, the SRTS generator is placed in the feedback loop of the PLL to synchronize on the incoming RTS. The SRTS generator consists of a divider 15, a four bit counter 17 and a register 16. The SRTS is in effect the remainder resulting from dividing the network clock fnx into the service clock fs divided by a suitable number, 3000 or 3008.

[0037] The maximum jitter allowed on f_s and f_{nx} is such that (f_{sx}/f_{nx})MOD16 remains constant under all circumstances. Otherwise, the basic principle of the SRTS method is violated. f_s comes from the PLL and is thereby clean enough. For f_{nx}, the user is responsible for the quality of the provided network clock. If it's not good enough, it must first be filtered with an external PLL.

[0038] The phase detector 10 must extract a phase difference value from its two input signals. There are two cases two consider. In one case the inputs are RTS values as inputs. In the other case the inputs are clock inputs. Both cases require different phase detectors, although certain parts can be shared.

[0039] In the case of RTS as input values, the output phaseword is the difference of the input values. However, because both input values come from counters, a modulo function is incorporated in these values. That gives false

has a limited accuracy.

[0050] The remaining value in the accumulator at a carry, the rest term, represents the exact phase error of the carry pulse with respect to an ideal signal. The error is maximally $1/f_{sys}$ and is the intrinsic jitter of the DCO. Increasing f_{sys} reduces the intrinsic jitter. The rest term can be used to correct the phase of the carry pulse, thereby reducing the intrinsic jitter. f_{sys} is high enough (> 64 MHz) to meet the jitter specs of 0.1 UI for DS1, E1 and J2 without much effort. An overview for a DCO with a clock frequency of 66 MHz is given in the table below.

DCO Freerun Clocks and Accuracies.			
Clock	f_s[MHz]	f_{dco}[MHz]	Accuracy[ppm]
DS1	1.544	12.352	0.05
E1	2.048	16.384	-0.13
C4M	4.096	16.384	-0.13
J2	6.312	25.284	-0.03
C8M	8.192	32.768	0.05

[0051] The jitter reduction circuit 12 is shown in Figure 13. This consists of a comparator 55 and a DQ flip-flop 56. The intrinsic jitter of the DCO output is normally 1/mclk. With the use of the negative edge of the master clock, the intrinsic jitter can be reduced to half of that. When the rest term is smaller than half the center frequency value, the carry pulse is delayed by half a master clock cycle. When the rest term is greater than or equals half the center frequency value the carry pulse is not delayed.

[0052] In the case that mclk = 66 MHz with a 40-60% duty cycle, the output jitter would be maximally 9 ns. The spectrum of the jitter ranges from 0 Hz to $f_{dco}/2$. With this jitter reduction circuit, the following intrinsic output jitter values would be achieved:

Intrinsic Output Jitter @ mclk = 66 MHz, 40-60% duty cycle.		
Clock	DCO Output Jitter [UI]	Reduced Output Jitter [UI]
DS1	0.02	0.01
E1	0.03	0.02
C4M	0.06	0.04
C8M	0.12	0.07
J2	0.09	0.06

[0053] The output divider 13 divides the DCO output frequency down to the required outputs. A standard counter is necessary to do the job. For the generation of the 8 kHz output, a loadable counter is needed to do the division from E1/DS1/J2 to 8 kHz. Some additional circuitry can be added to generate the right frame pulse format.

[0054] The described clock recovery circuit is efficient and versatile, capable of operating in four modes. It can be used with or without multiple selectable center frequencies, with or without a center frequency programmed as a register from an microprocessor, with or without a mode where the integrating register can be read by a microprocessor, with or without a mode where a microprocessor can adjust the center frequency based on an algorithm tied to the values read from the integration register (i.e. a mode where a microprocessor is used as a controller of the feedback loop of the PLL, giving longer time constants than can easily be achieved in hardware), with or without a jitter reduction circuit, with different master clock (MCLK) frequencies, and with a jitter reduction circuit based on the negative clock edge, or with a jitter reduction circuit based on a tapped delay line. Various PLL parameters can be changed without departing from the spirit of the present invention, including: center frequency, locking range, input jitter tolerance, jitter transfer function, max phase slope. It can be used with or without automatic switch-over to holdover passed on validity of received SRTS nibbles, and with or without automatic switch-over to holdover passed on underun due to lost ATM connection.

[0055] It can also be used for mode conversion, as an intermediate node, to convert received adaptive clocking to transmit SRTS clocking, using the circuit of Figure 5, by making the input the adaptive input. It can be used for T1 to E1 conversion with an extra circuit, and it is also applicable to DS3 and E3 rates. It can also work in conjunction with another PLL (internal or external to the IC).

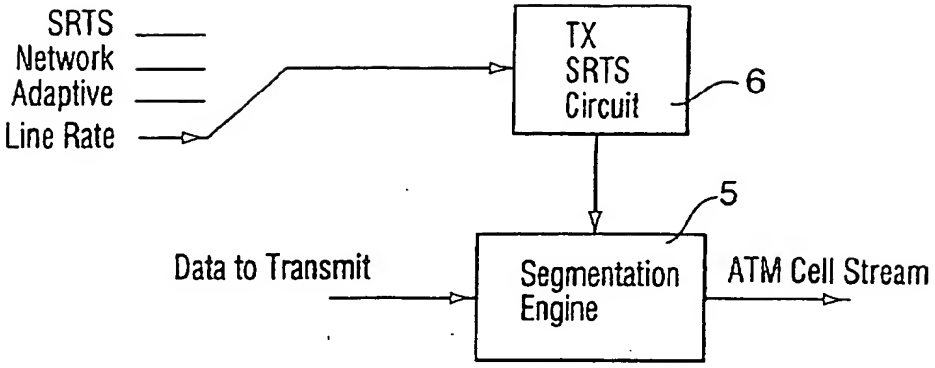

FIG. 4

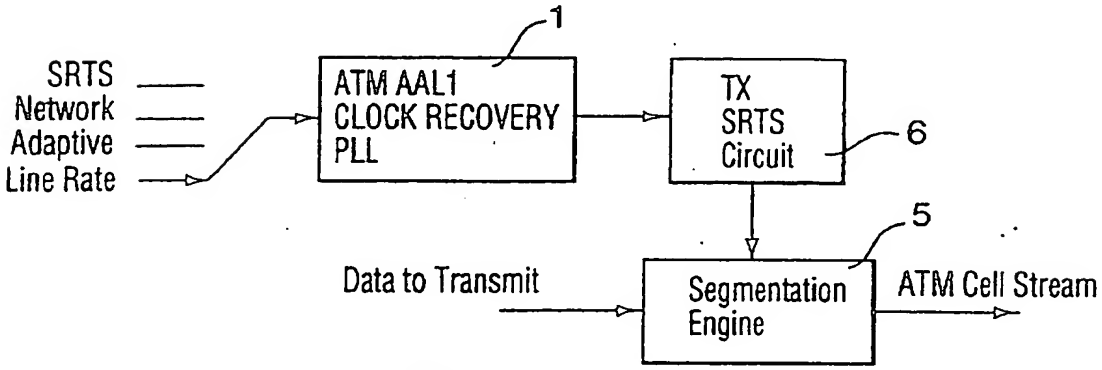

FIG. 5

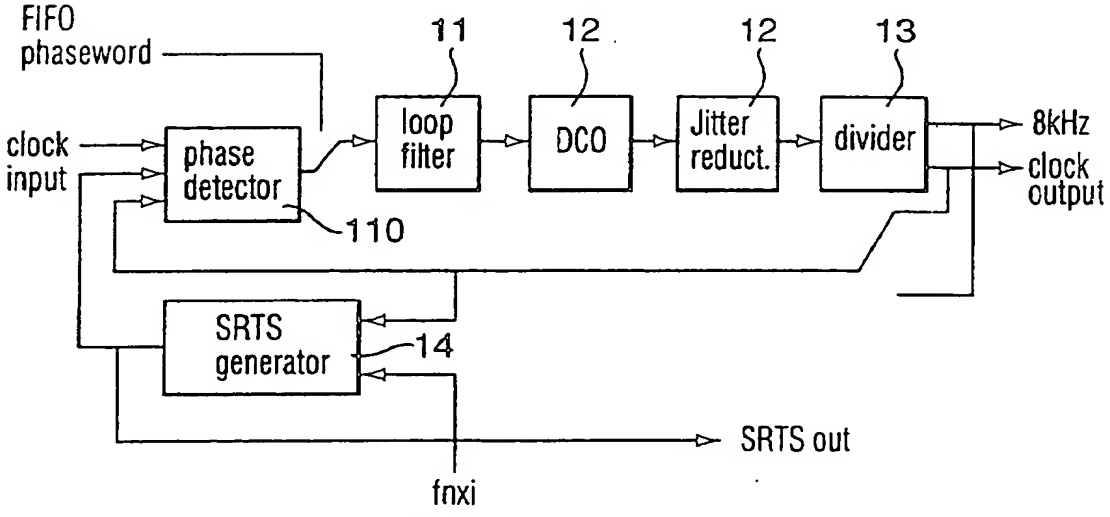

FIG. 6

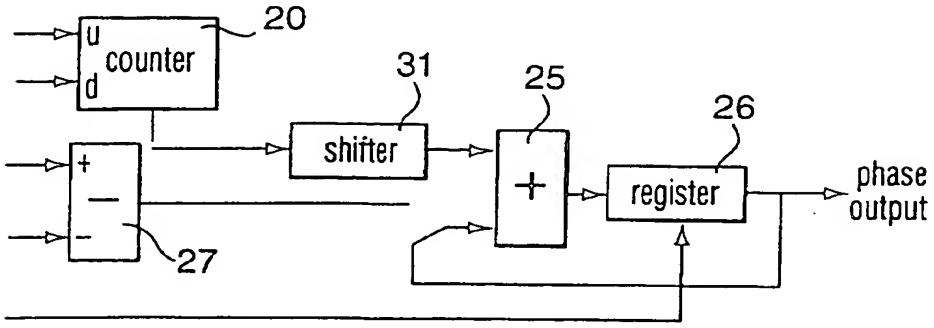

FIG. 10

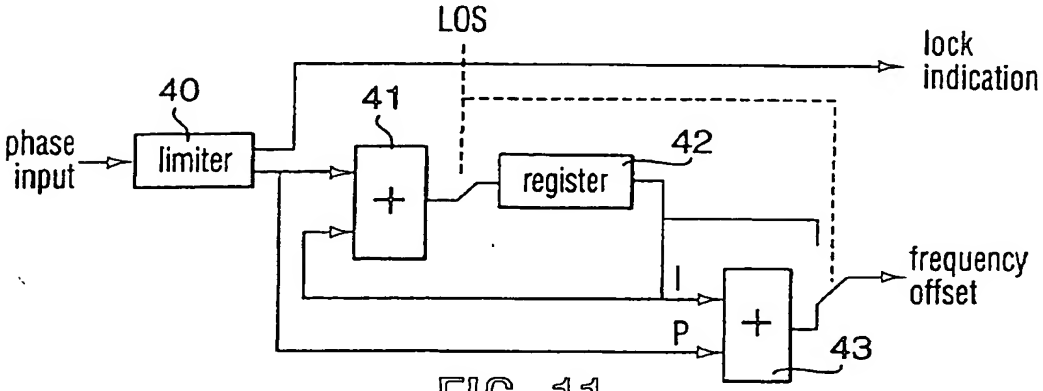

FIG. 11

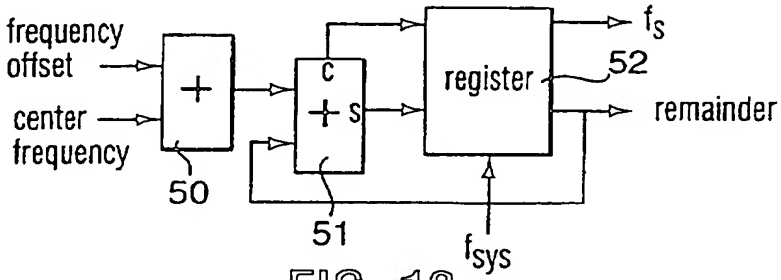

FIG. 12

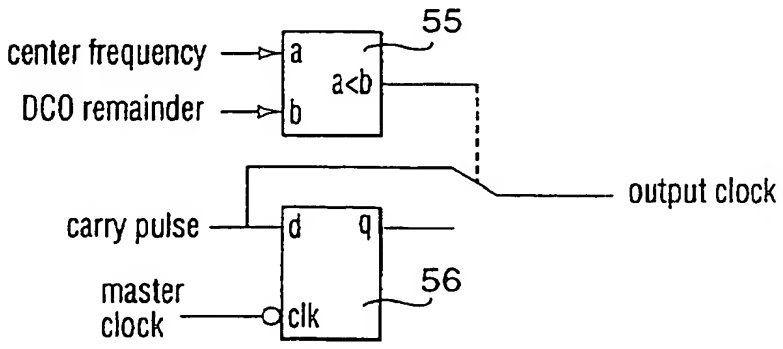

FIG. 13